Noise Optimisation of Charge Sensitive Amplifier

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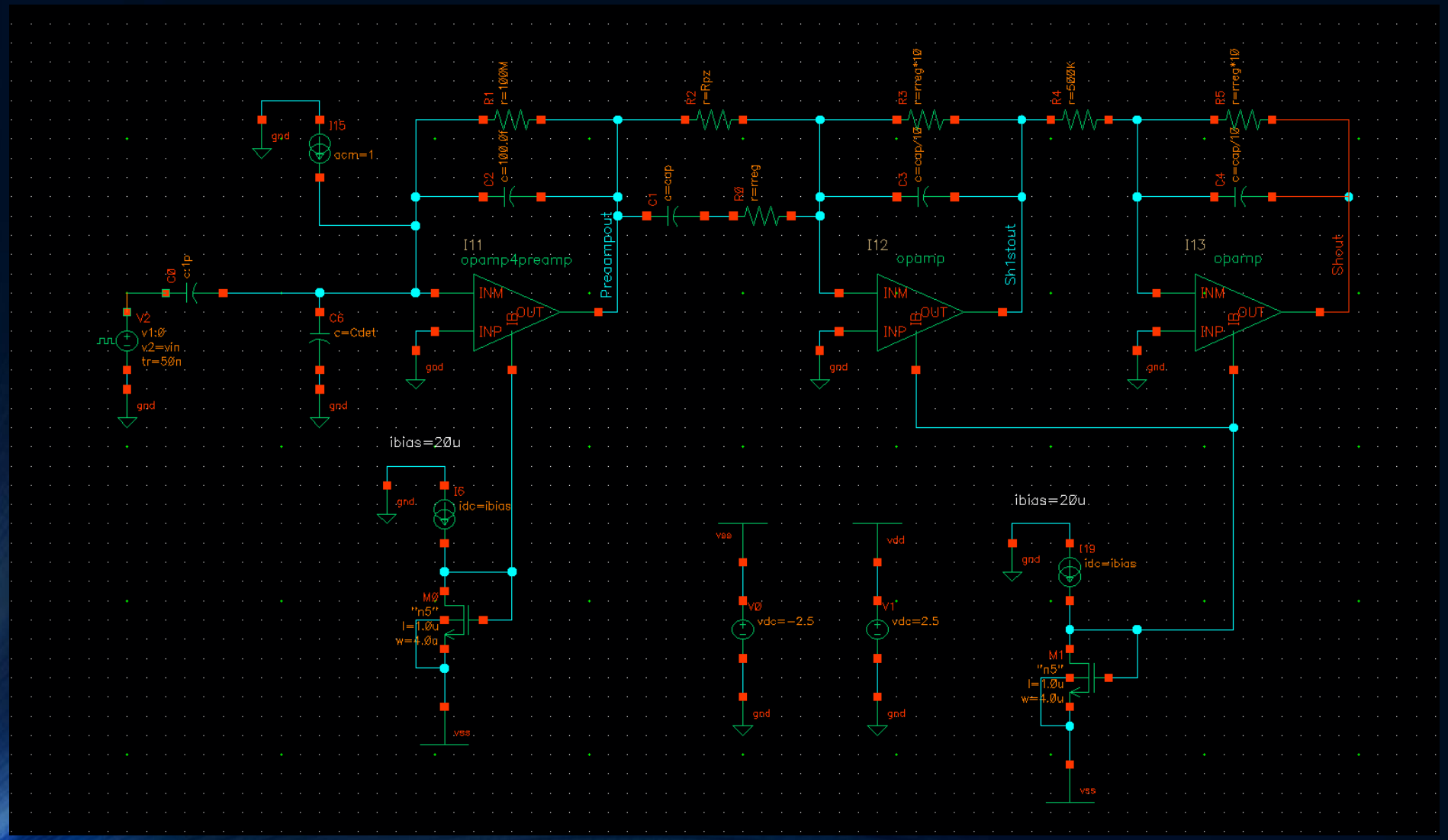
Introduction and Motivation

- The signal from the detector has to be shaped into a Semi-Gaussian form to facilitate further processing.
- For a Pixel detector, each pixel requires a separate wave shaping circuit; hundreds of wave shaping circuits have to be packed into a compact space. Hence the need to use an ASIC chip for the same.
- The first stage of signal conditioning is the Charge Sensitive Amplifier or Preamplifier. It is important to have as little noise in the preamplifier as possible to obtain a good Signal to Noise Ratio.
- A proposed charge sensitive amplifier was compared to the reference CSA.

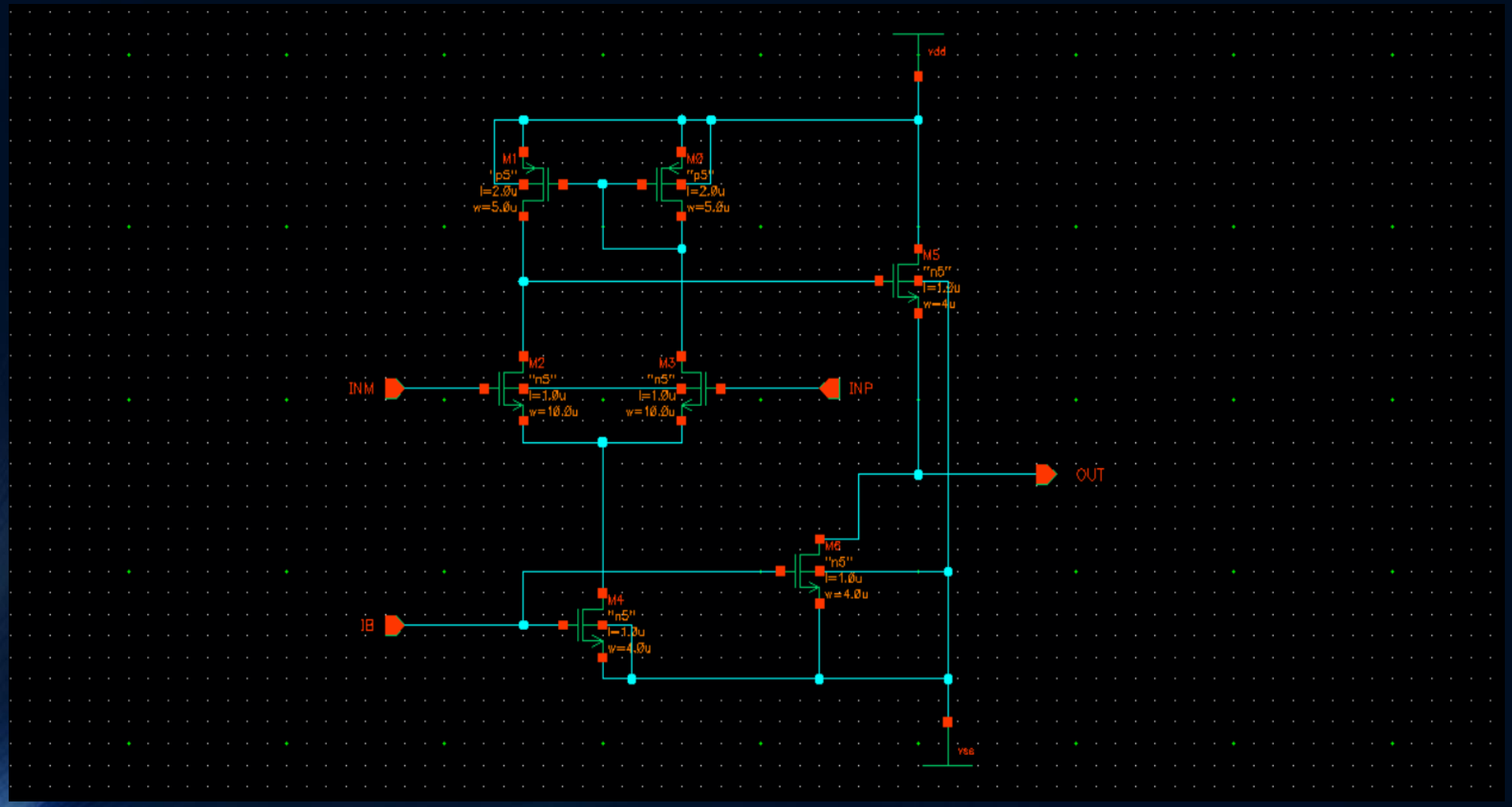
Learning Objectives

- Learnt to use the CAD tool for making ASIC schematic, layout and simulation.
- Studied the transient response, AC analysis, DC analysis and noise tools in the Cadence software.
- Learnt about noise characterization, dependence of noise on bias currents and detector capacitance.
- Learnt about the dependence of noise on transistor on channel width and multiplicity (M value).
- Learnt about the precise LPE simulation for ASIC chips.

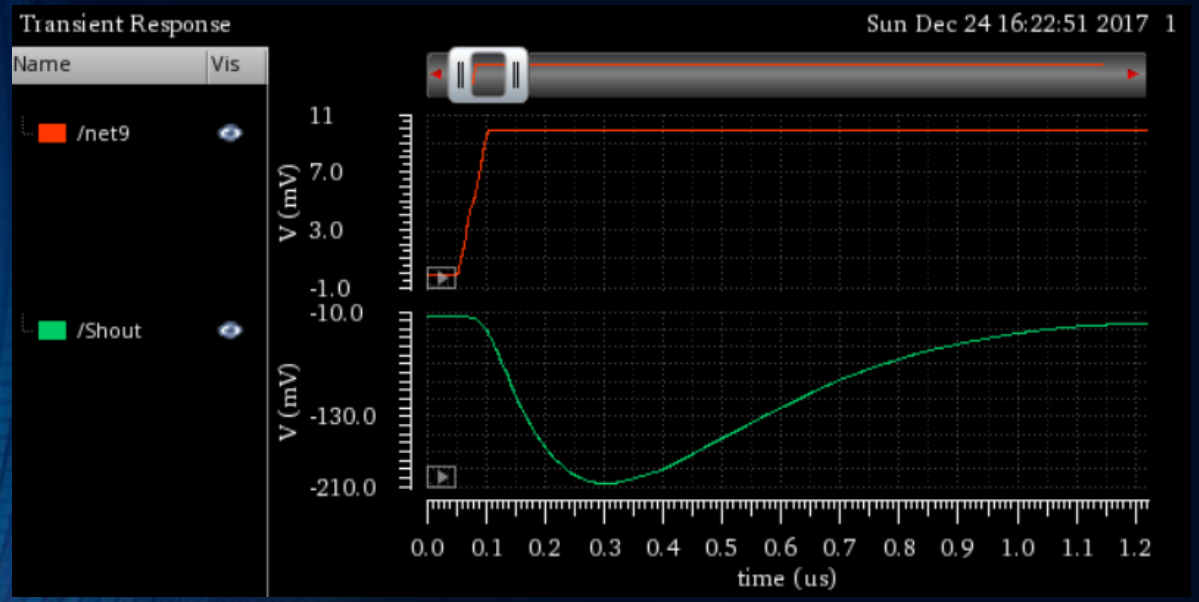
Reference wave shaping circuit.



OpAmp Design

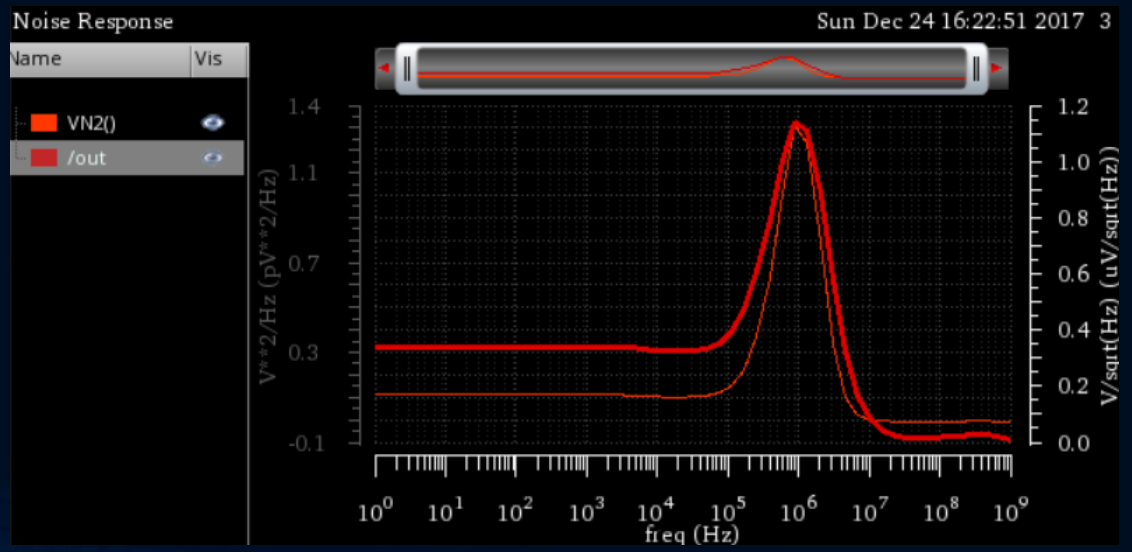


Characteristics of Reference Circuit



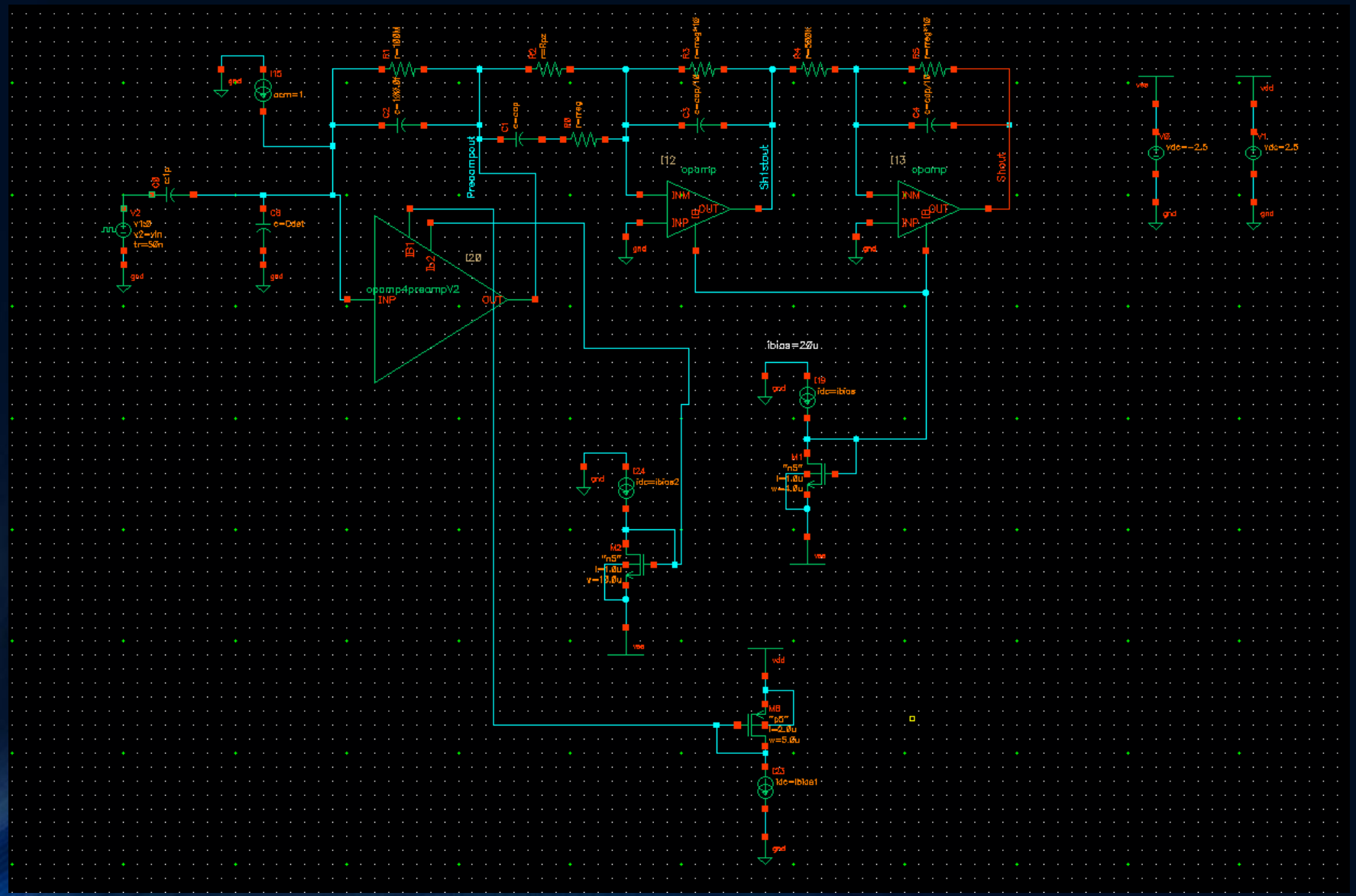
Transient Response

Equivalent Noise Charge: **644**
Detector Capacitance: 1pF

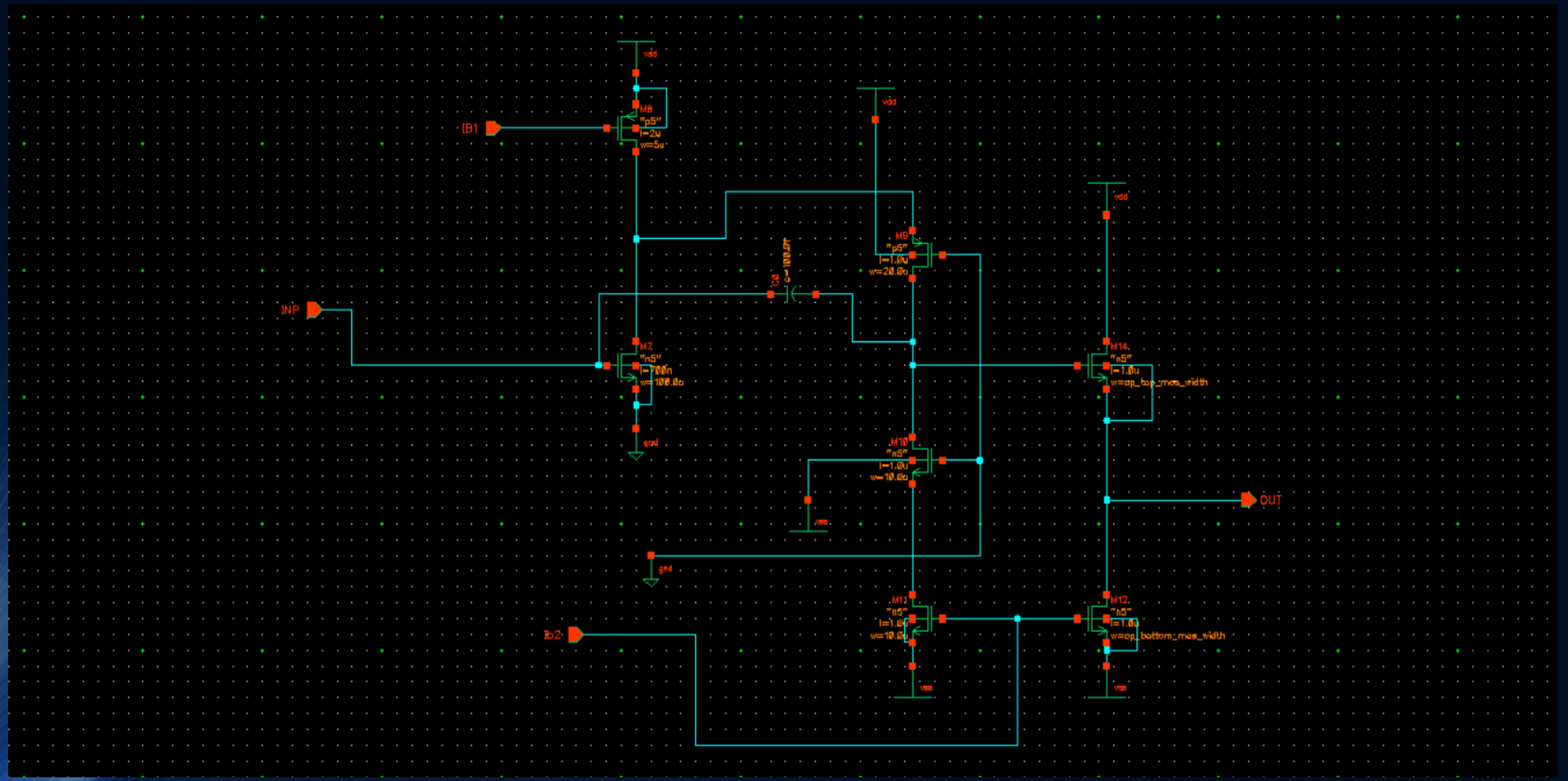


Noise Spectrum

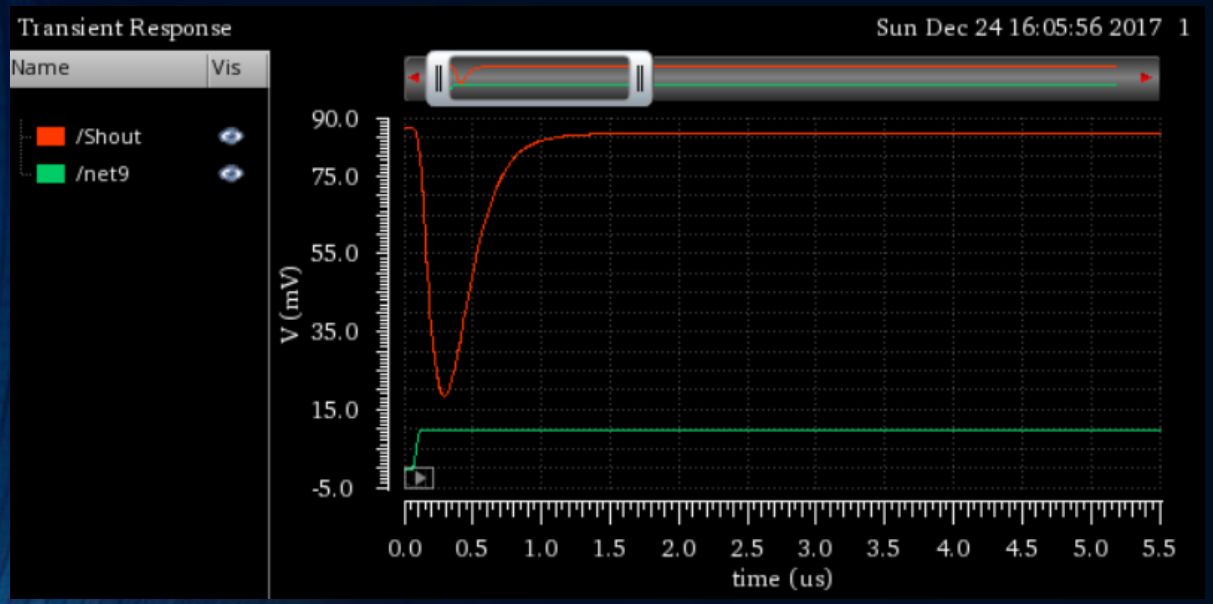
Testing of New Single-Ended amplifier



Proposed OpAmp Design

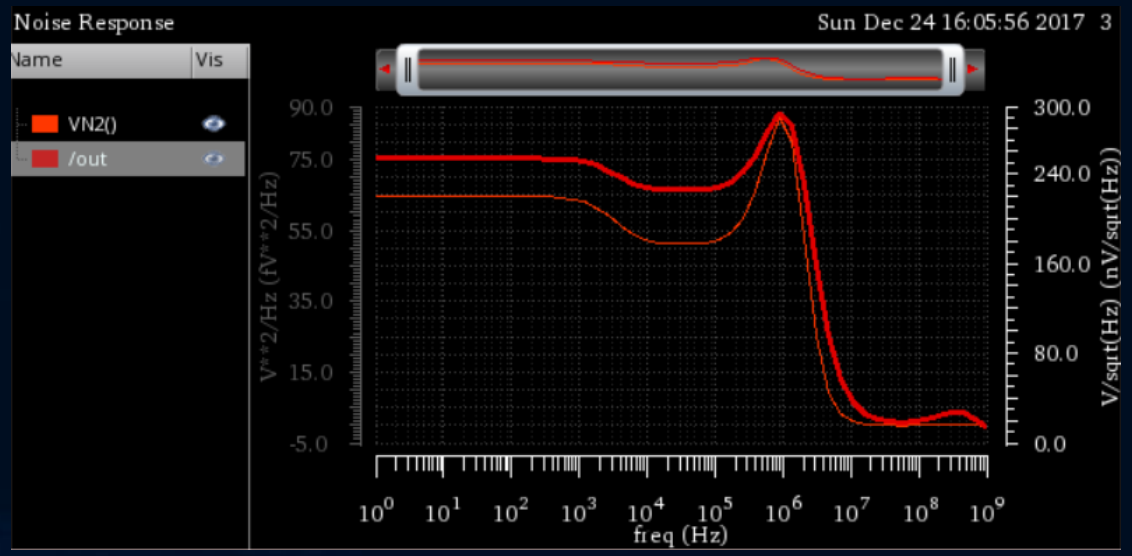


Characteristics of Proposed Circuit



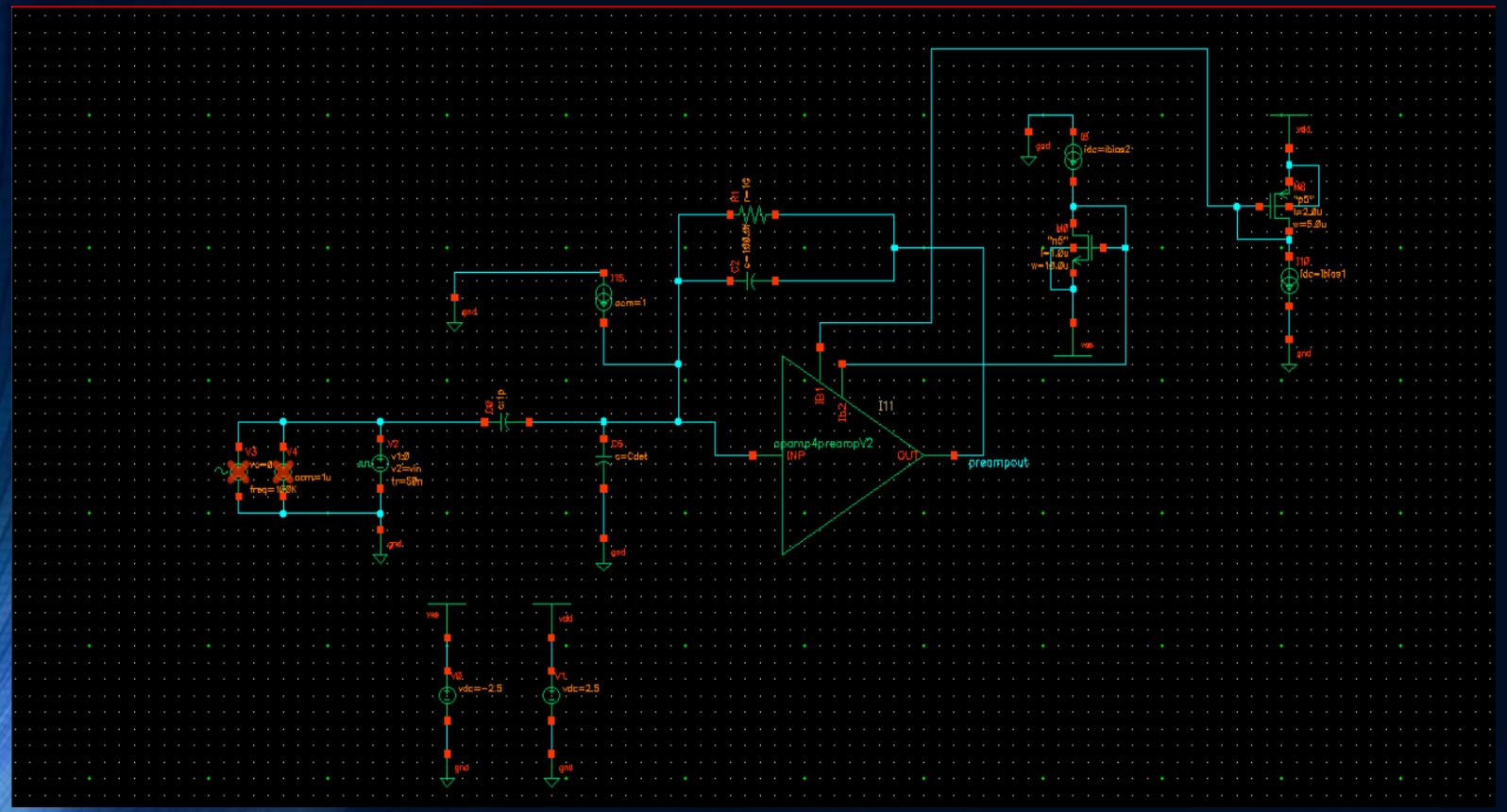
Transient Response

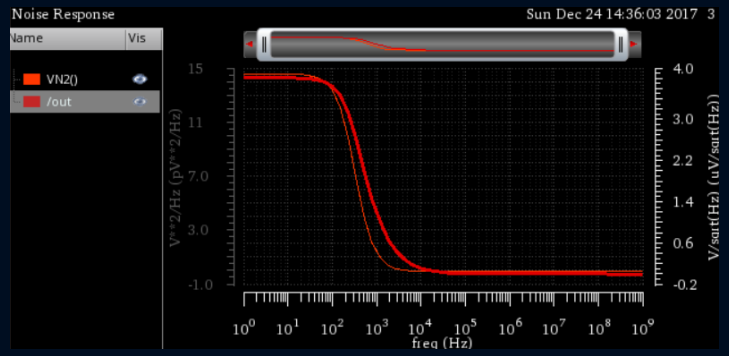
Equivalent Noise Charge: **815**
Detector Capacitance: 1pF

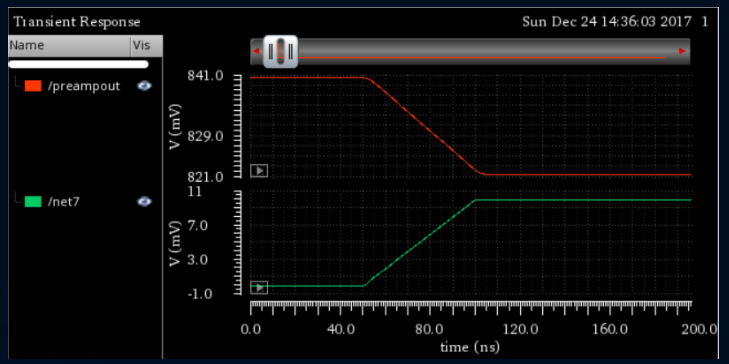


Noise Spectrum

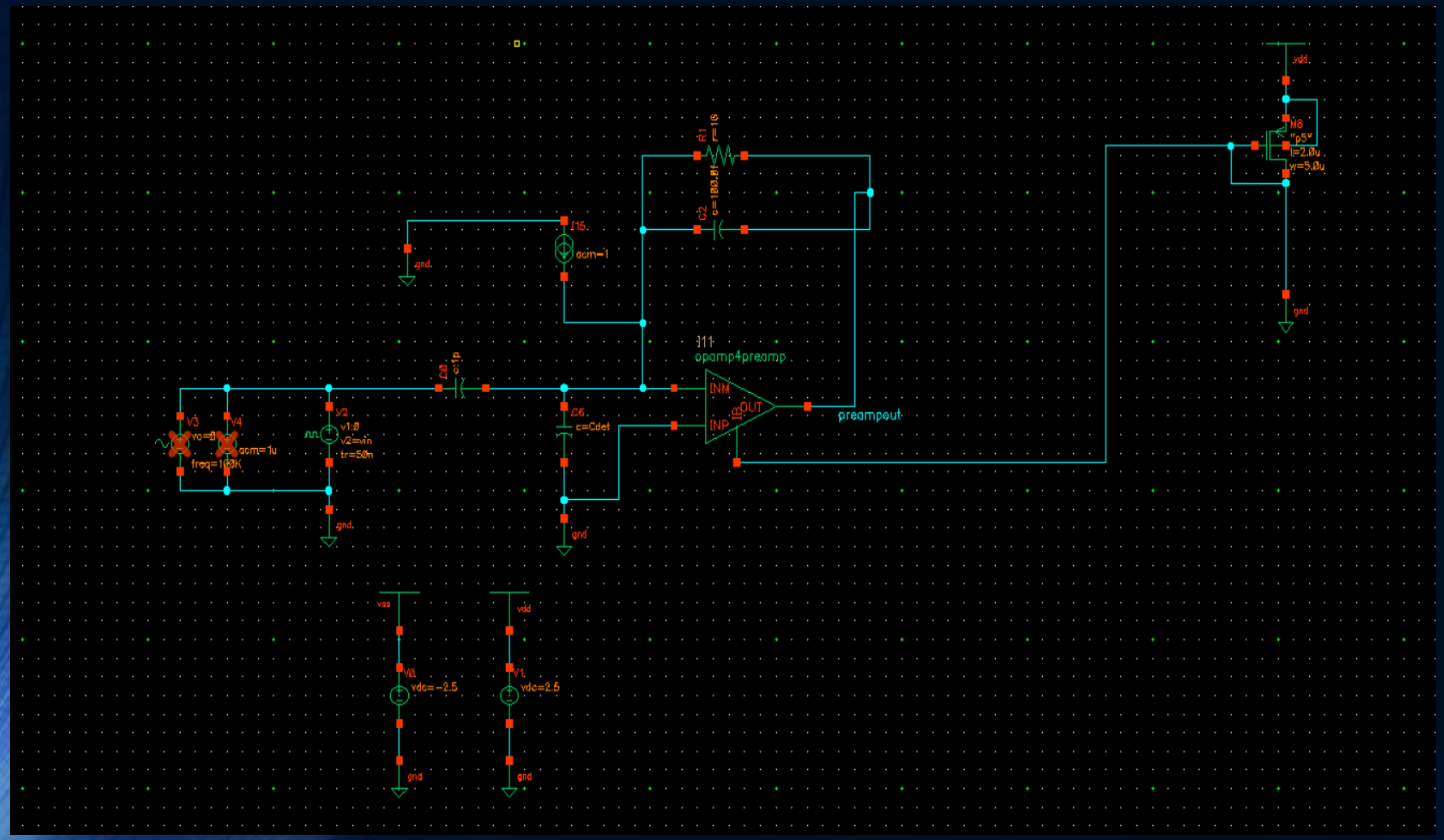
Output of Proposed Charge Sensitive amplifier

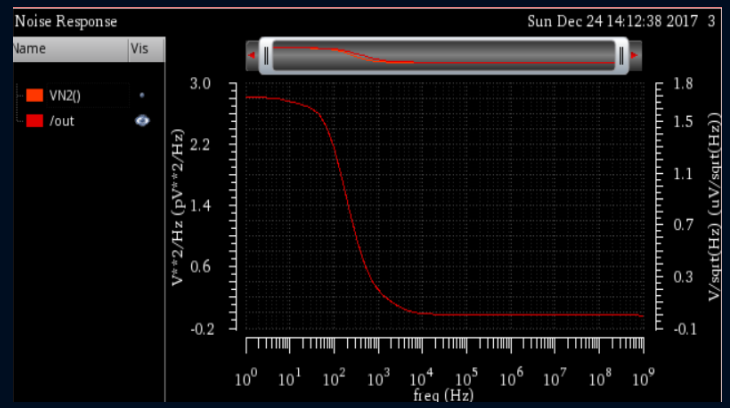


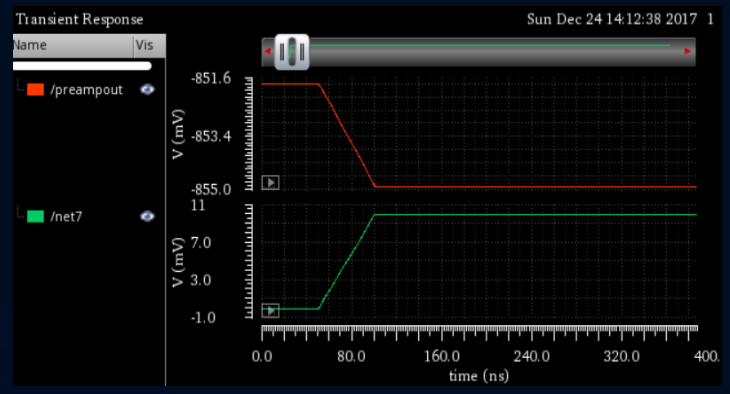




Output of Reference Charge Sensitive amplifier







Comparison of new amplifier with reference Opamp

- The proposed design was found to have slightly higher noise than the reference design.
- The noise performance may be improved by adjusting the bias currents.
- Using higher M value for transistors in the ASIC design or widening the conduction channels may lead to better noise performance.

Control and Characterisation of Pixel ASIC chip using FPGA

Supervised by Dr. Tetsuichi Kishishita,
IPNS, KEK

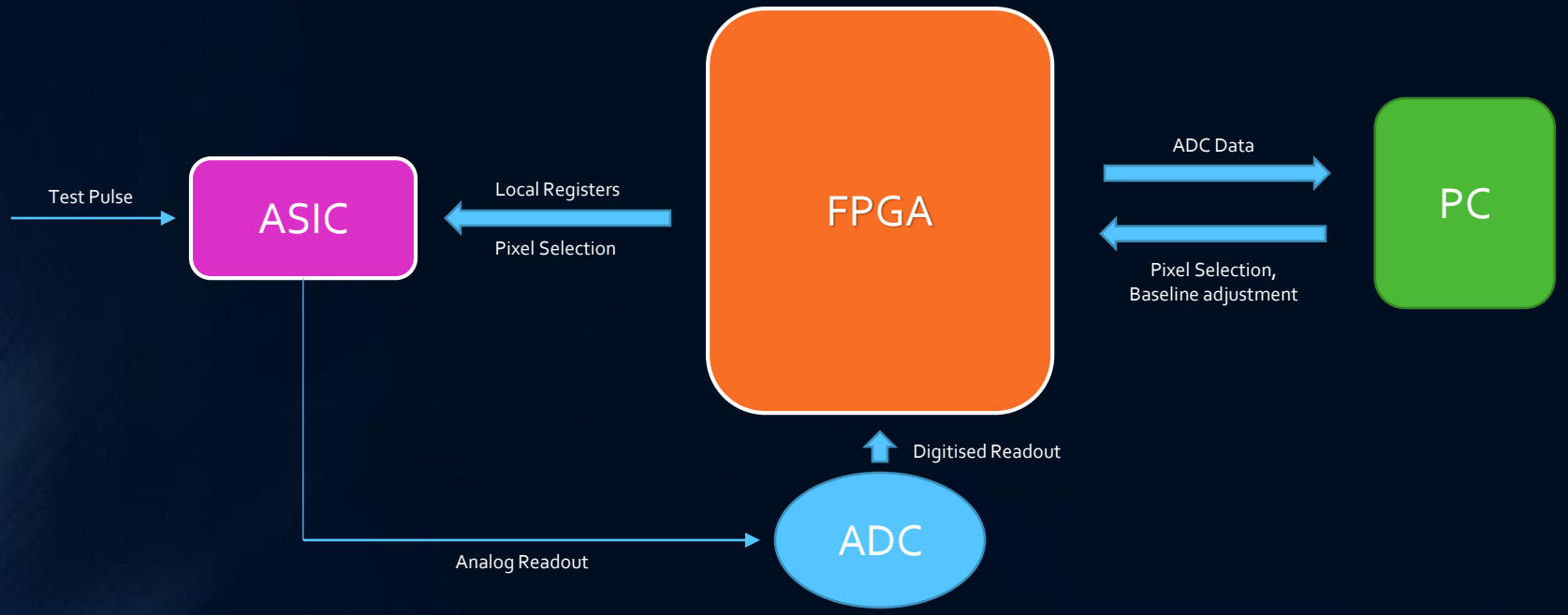
Introduction and Motivation

- An FPGA was used to control a two dimensional analog front end ASIC for hybrid pixel detectors.
- Each among the 144 pixels had a charge-sensitive amplifier, shaper, comparator, and peak hold circuit.
- The pixel selection for setup and readout is done using peripheral daisy-chained registers.
- The baseline adjustment, testing mode and enabling/disabling noisy channels were implemented using local registers in each pixel.
- An FPGA was used to set the proper values for the registers and for reading data.

Learning Objectives

- Studied the scaleable design of a mixed signal ASIC chip.
- Learnt about trigger systems and the self-triggering mechanism employed in a Pixel detector.
- Studied the serial data readout mechanism for a large pixel array.
- Studied the waveshaping and peak holding circuits to facilitate data readout by ADC.
- Familiarised with the Xilinx design and simulation environment.
- Implemented a UART transmitter and receiver on FPGA for communication with PC.

Functional block diagram



Block Diagram of the ASIC Chip

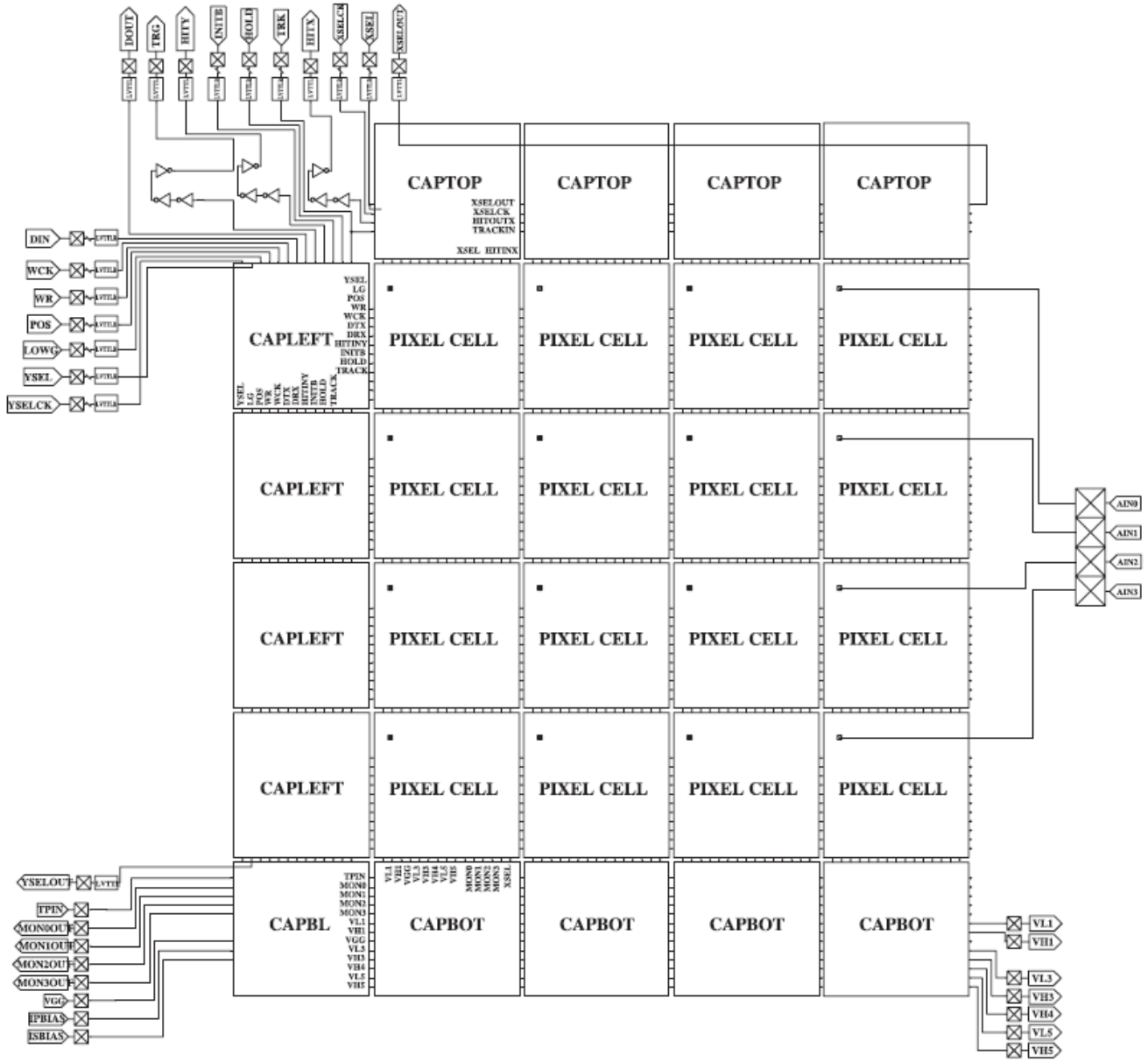
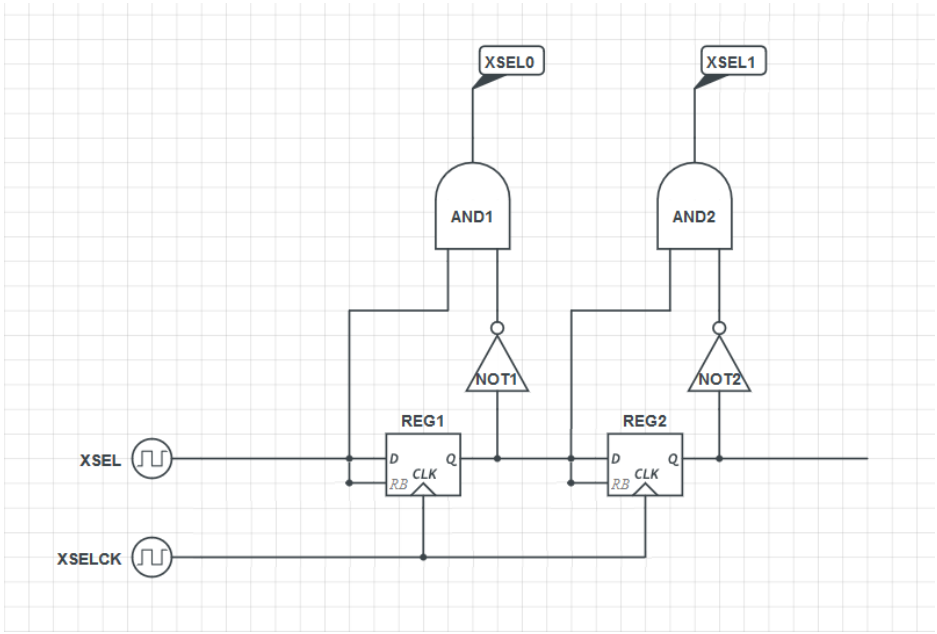
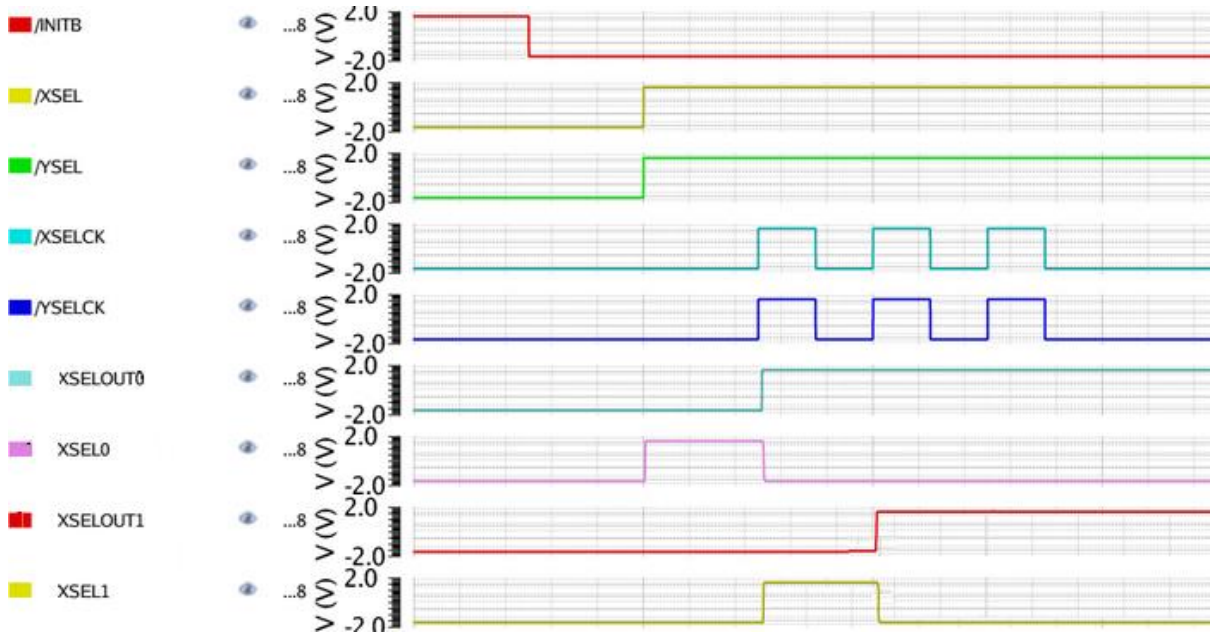


Fig. 2. Block diagram of the ASIC. Bias voltages are supplied from the bottom module. Shift registers used for pixel selects are contained in CAPTOP and CAPLEFT modules. Analog inputs of the outer four pixel cells are connected to bonding pads.

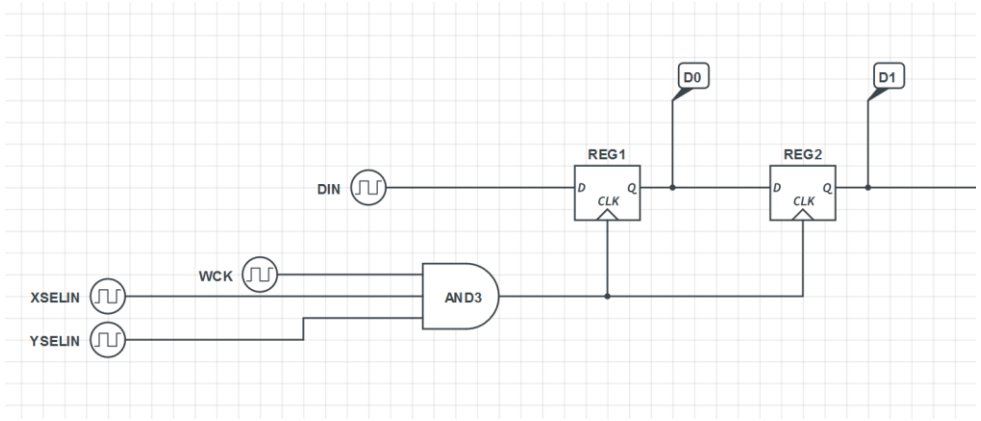
Pixel Selection

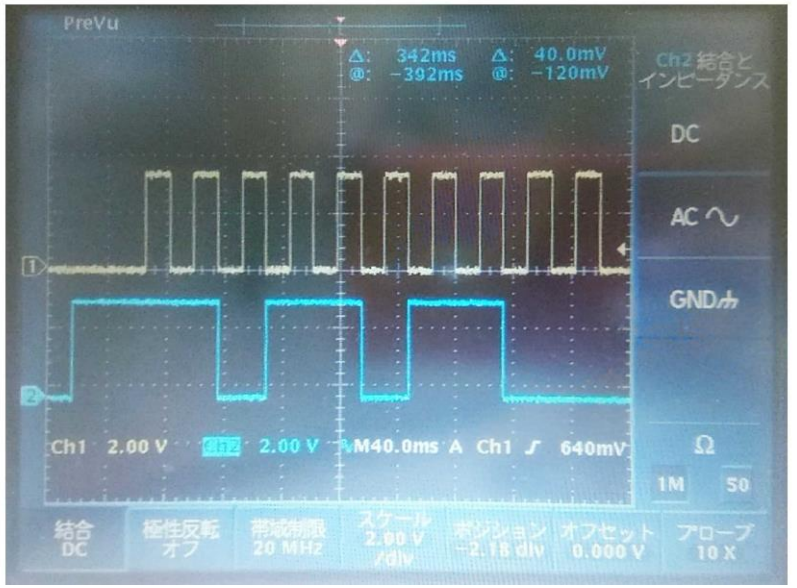




This ensures that at a time, only one pixel can be selected

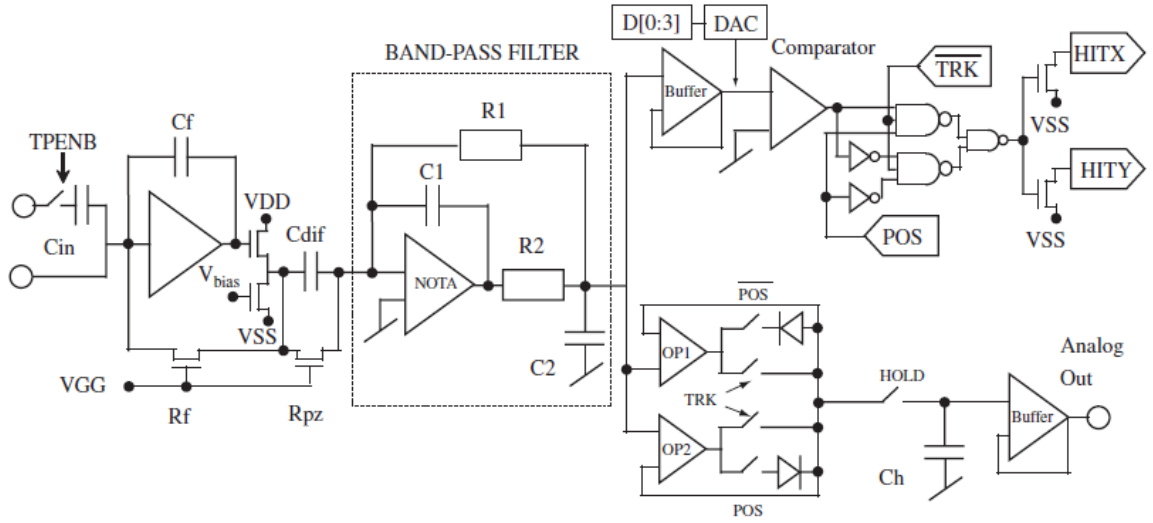
Local Registers





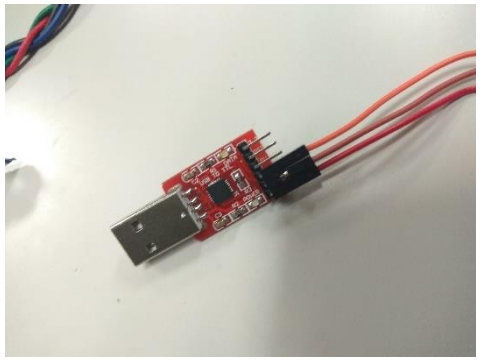
Analog Circuit

- POS decides the polarity of signal
- TRK activates the peak hold circuit
- TPENB in the local register sets the pixel in testing mode.
- HIT signals can be used for the trigger mechanism
- When waiting for a signal, track has to be low, i.e. peak hold circuit is active.
- Once hit signal is obtained, peak hold circuit has to be reset after reading by ADC by setting track to high, allowing the capacitor to discharge.

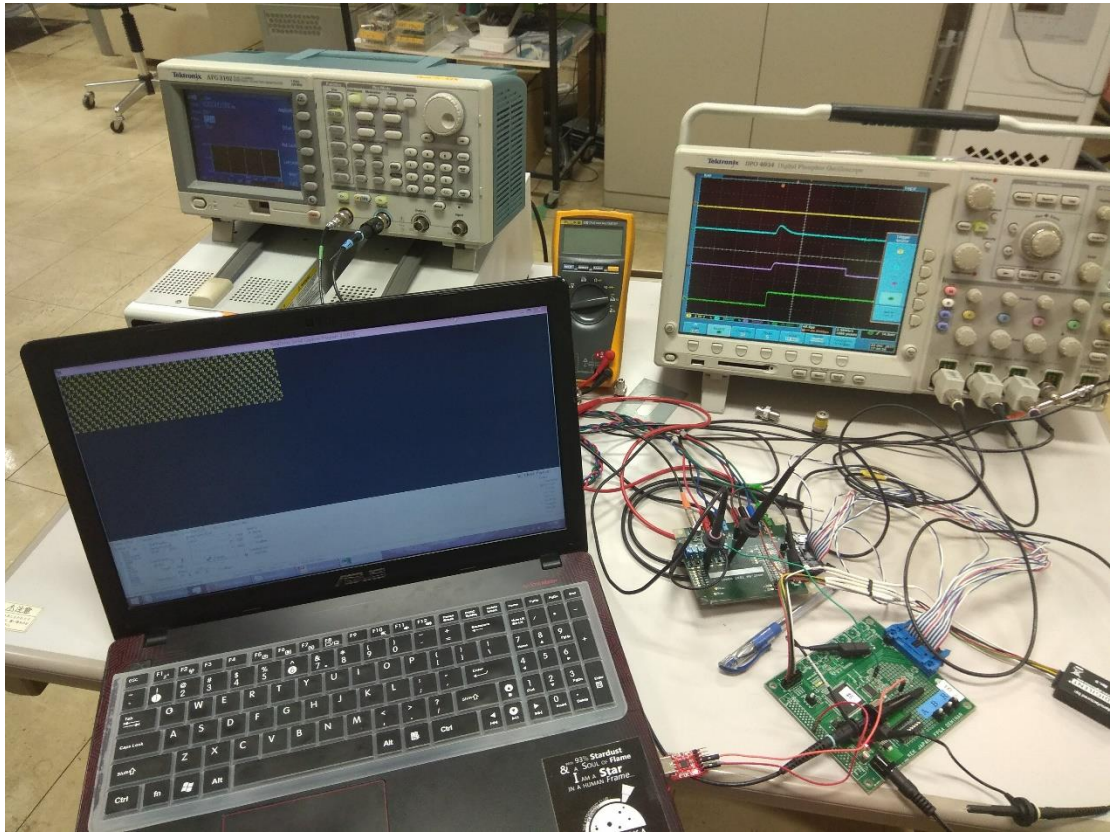


Setup

- Test pulse generated by Function Generator
- TPENB is set to LOW.
- UART protocol was implemented in FPGA for communicating with PC.
- Used Realterm to monitor data.



UART converter for communication with PC



Results

Trigger

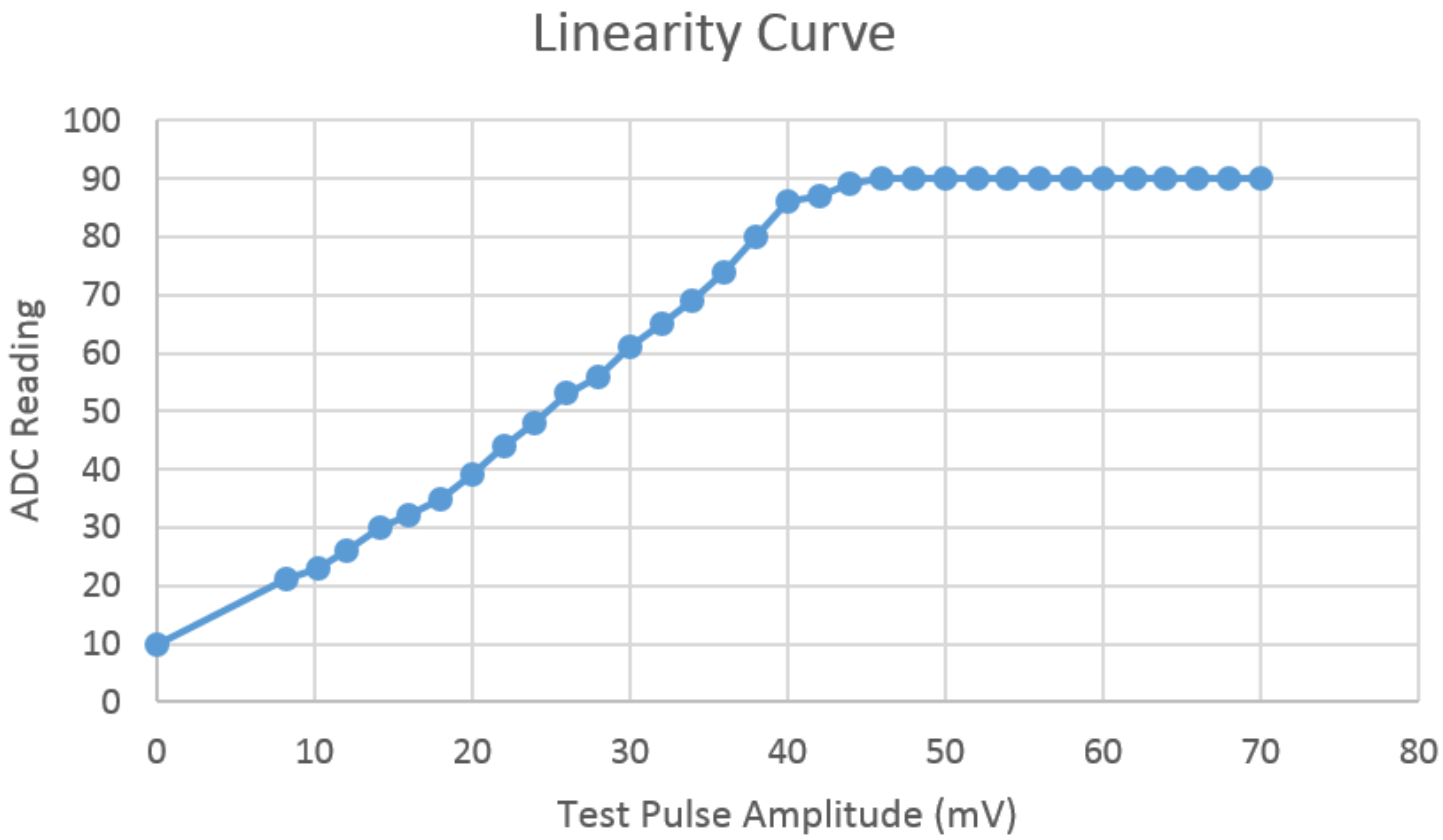
After Band-pass filter

Peak Hold Circuit Output

Test Pulse

Results

- The output was found to be linear with input for a wide range of input amplitude.
(ADC Reading – 1 unit ~ 8.7mV)



A note of thanks to Tanaka-san, Ichi-san, Ono-san and all others who made this cultural and educational exchange possible.

thank you!